Arjun Nair

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Education

Bachelor of Science in Computer and Electrical Engineering, Double Major Aug 2019 – May 2024
North Carolina State University *Raleigh, NC*

Relevant Coursework

- Compiler Optimization and Scheduling, Neural Nets, Intro to Nano Science & Technology, ASIC & FPGA Design in Verilog, Digital System Design in Verilog, Embedded Systems, Computer Systems Programming, Data Structures and OOP, Physics of Microelectronics

Technical Skills

Languages: C/C++, Embedded C, Python, Verilog, VHDL, Git, Assembly, MATLAB, HTML
Circuit Design: Altium Designer, Mentor Graphics Xpedition, PSpice, PowerDC, Logic Design, Verification Testing

Work Experience

Advanced Micro Devices (AMD) Inc. Jan 2024 - June 2024
Signal Integrity Intern *Austin, TX*

- Developed **Python-based CAD tools** to assist **Signal Integrity** and **Power Integrity** engineers
- Launched an **auto-routing tool** project using **A* algorithm** for breakout routing in memory channels
- Created a **power plane feasibility tool** for Power Through Hole (PTH) pattern implementation
- Automated generation of **transition layers** for **multi-layer power planes**, reducing engineering time from **1-2 months** to **2-3 days**
- Applied **Cadence SKILL** to allow users to easily transfer layout information from the Python tool to **Cadence Allegro**

Intel Corporation May 2022 - Dec 2022
R&D IC Package Design Engineer Intern *Chandler, AZ*

- Assisted in **designing** and **routing** the **PCB** package layout for **DDR**, **UCIe** and various other **Intel packages**
- Performed microelectronic **IC** electrical **modeling** and **simulation** using tools such as Xpedition, PowerDC
- Designed **manufacturing drafts** (die/die bonding diagrams, packing specs, mark specs, Bill of Materials list, etc)
- Collaborated with relative **teams**, **clients** and **vendors** to support **production** and establish problem specifications

Edwards Vacuum May 2021 – Aug 2021
Electrical Engineering Intern *Chelmsford, MA*

- **Designed** and printed circuit board **schematics** in **Altium** used in conjunction with **various product lines**
- Built **test fixtures** to perform Reliability Demonstration Testing on **electrical sub-assemblies**
- Performed **Design Verification Testing** (DVT) on various components using a variety of **lab equipment**
- Applied **EMIC** principles to ensure electronics were compliant with **industry standards**

Projects

Face Detection and Student Engagement System | *Python, Machine Learning, PCA* May 2023

- Developed as a Final Project in a **Neural Networks** class, presented at the **Machine Learning Symposium**
- Implemented an Eigenface and Principal Component Analysis (PCA) approach for **face detection**, training a model using 10 images and storing this training data (facial features)
- Integrated a pre-trained engagement detection model to **determine student engagement levels** and **generate student engagement reports** for instructors

Multi-Stage Neural Network | *Verilog* Aug 2022

- Implemented a hardware-based multi-stage **neural network** in **Verilog**, including a convolutional layer, a fully connected layer and a max pooling layer
- Applied **algorithms** to efficiently read and write data to and from input and output **SRAMs**
- System generates output matrix which can be used to **classify** objects
- **Optimized** design to ensure **top 1%** in cycle-count and area among **300** classmates

Activities & Awards

Intel Department Recognition Award (For work on **Meteor Lake** DDR routing) Nov 2022
IEEE at NCSU (Member) Jan 2022 - May 2024
Rock Climbing Club (Member) Aug 2021 - May 2024